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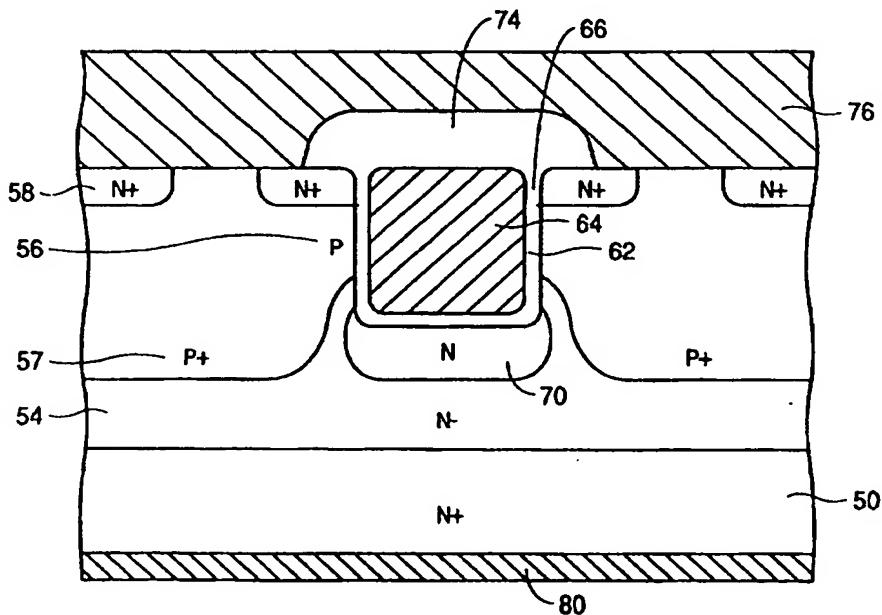
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(54) Title: HIGH DENSITY TRENCH DMOS TRANSISTOR WITH TRENCH BOTTOM IMPLANT



(57) Abstract

A trenched DMOS transistor overcomes the problem of a parasitic JFET at the trench bottom (caused by deep body regions (57) extending deeper than the trench) by providing a doped trench (62) and extending into the surrounding drift region (54). This trench bottom implant region (70) has the same doping type, but is more highly doped, than the surrounding drift region (54). The trench bottom implant region (70) significantly reduces the parasitic JFET resistance by optimizing the trench bottom implant dose, without creating reliability problems.

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HIGH DENSITY TRENCH DMOS TRANSISTOR WITH
TRENCH BOTTOM IMPLANT

5 BACKGROUND OF THE INVENTION

Field of the Invention

This invention relates to transistors and more specifically to a high density trenched DMOS transistor.

10 Description of the Prior Art

DMOS (diffused metal oxide semiconductor) transistors are well known. Typically these 15 transistors are used in integrated circuits or for power transistors. Some DMOS transistors are trenched transistors; a conductive gate electrode, typically polycrystalline silicon (polysilicon), is located in a trench in the transistor substrate, and the sidewalls 20 and bottom of the trench are insulated with silicon dioxide. The trenched structure increases transistor density by reducing the chip surface area consumed by the polysilicon gate of each transistor. Typically such transistors are used in low to medium voltage 25 applications, and each transistor includes a large number (thousands) of cells. Each cell is defined by a source region diffused into the substrate and by the gate electrode trenches.

The provision of the trenches advantageously 30 increases cell density and also reduces the undesirable parasitic JFET (junction field effect transistor) resistance which typically is present between adjacent cells. The parasitic JFET resistance is one component 35 of the total on-state resistance, $R_{DS(on)}$, which is characteristic of such transistors in their conductive (on) state; it is desirable to minimize the on-resistance.

However, trenches do not completely eliminate parasitic JFET resistance. When cell density is high in a trenched DMOS transistor, a new parasitic JFET phenomenon gradually appears between the adjacent deep body P+ regions which extend alongside the trench and are typically used to protect the trench regions and ensure reliability. Unfortunately, this new JFET resistance becomes a significant component of on-resistance as cell density increases.

By design, avalanche breakdown occurs in the P+ doped regions away from the trench bottom. In a typical DMOS transistor having a trenched gate electrode, in order to avoid destructive breakdown occurring at the bottom of the trench into the underlying drain region, the deep body P+ region extends deeper than does the bottom of the trench. Rather than the destructive breakdown occurring at the trench bottom, therefore instead the avalanche breakdown occurs from the lowest portion of this deep body P+ region into the underlying relatively nearby drain region.

It is well known that the trenched DMOS transistor structure is superior to a planar DMOS transistor in terms of drain-source specific on-resistance, which is resistance times the cross-sectional area of the substrate carrying the current. The JFET resistance, inherent in planar DMOS transistors, is significantly reduced and cell density is enhanced by reducing the length of the gate electrode.

An example of a planar DMOS transistor is disclosed in Lidow et al. U.S. Patent No. 4,642,666 issued February 10, 1987 which discloses as shown in present Figure 1 (similar to Figure 2 of Lidow et al.) a high power MOSFET in which two laterally spaced sources each supply current through respective channels in one surface of a semiconductor chip, controlled by

the same gate. The epitaxially deposited semiconductor material immediately adjacent and beneath the gate and in the path from the sources to the drain is of relatively high conductivity (is highly doped), thereby 5 substantially reducing the on-resistance of the device without affecting the device breakdown voltage.

Thus as shown in present Figure 1, the Lidow et al. MOSFET is formed in a chip of monocrystalline silicon 20. Two source electrodes 22 and 23 are 10 separated by a metallized gate electrode 24 which is fixed to but spaced apart from the semiconductor device surface by a silicon dioxide layer 25. Each of source electrodes 22 and 23 supply current to a drain electrode 26 which is fixed to the bottom of the wafer. 15 An N- doped epitaxial layer is deposited on N+ doped substrate 20. P+ doped regions 30 and 31 each include a curved lower portion which serves as a deep body region. Two N+ regions 32 and 33 are formed at the source electrodes 22 and 23 respectively and define, 20 with the P doped regions 34 and 35, channel regions 36 and 37 which are disposed beneath the gate oxide 25 and can be inverted from P-type to N-type by the appropriate application of a bias voltage to the gate 24 in order to permit conduction from the source 25 electrodes 22 and 23 through the inversion layers into the central region disposed beneath the gate 24 and then to the drain electrode 26. (Reference numbers used herein referring to Figure 1 differ somewhat from those in the Lidow et al. disclosure.)

30 In the central region beneath the gate 24 is located a highly conductive N+ doped region 40 disposed immediately beneath the gate oxide 25. The N+ region 40 has a depth of about 4 μ m. Region 40 is relatively highly doped compared to the N- doped region 35 immediately beneath it. By making region 40 of relatively highly conductive N+ material by a diffusion

or other operation, the device characteristics are significantly improved and the forward on-resistance of the device is reduced by a factor greater than two. Provision of the high conductivity region 40 does not 5 interfere with the reverse voltage characteristics of the device. Accordingly the forward on-resistance of the ultimate high power switching device is significantly reduced.

However the Lidow et al. device is a planar (non-trenched) transistor structure and has the accompanying 10 drawbacks of relatively low cell density and relatively high inherent JFET resistance.

SUMMARY

In accordance with the present invention, a 15 trenched DMOS transistor includes a trench bottom implant region which is of the same doping type, but more heavily doped, than is the surrounding drift region. Thereby, the doping concentration in the area at the trench bottom is increased. This results in significant reduction of the JFET resistance otherwise 20 characteristic of trenched DMOS transistors, by optimizing the concentration of the trench bottom implant region, without creating any reliability 25 problems. Thus, in effect the new parasitic JFET observed by the present inventors at the trench bottom (where the deep body regions extend deeper than the trench) is substantially eliminated. Also, in accordance with the invention, trench corner electrical 30 breakdown at high voltage is avoided, and avalanche still occurs in the P+ regions. The trench bottom implant region is fabricated in one embodiment by etching the trench in the substrate, lining the trench with oxide, and then performing a blanket implant of a 35 dopant at a vertical angle, to form a doped region extending from the bottom of the trench into the

surrounding drift region. This is accomplished prior to formation of the gate electrode itself in the trench, and also prior to forming the source, body and deep body regions.

5 U.S. Patent No. 4,983,160 issued January 9, 1990, to Blanchard depicts (see Figure 3) a trenched DMOS transistor with an N+ doped region at the lower sides and bottom of the trench. The purpose of this N+ region is to increase breakdown voltage. Hence the 10 doping level of this N+ region is fairly high. Moreover, in this transistor the P+ body regions are much shallower than is the trench, hence there being no parasitic JFET problem.

15 BRIEF DESCRIPTION OF THE DRAWINGS

Figure 1 shows a prior art planar MOSFET.

Figure 2 shows a transistor in accordance with the present invention.

Figures 3A to 3D shows steps for forming a 20 transistor in accordance with the present invention.

DETAILED DESCRIPTION OF THE PREFERRED EMBODIMENTS

Figure 2 shows a cross-section of a transistor in accordance with the present invention. This cross-section is drawn conventionally and shows only portions 25 of several cells of a typical transistor, which may include thousands of such cells. However, a single cell transistor is also possible. Also, while the present disclosure is directed to a transistor having 30 an N type (N doped) substrate, a P type (P doped) body region and an N type source region, it is to be understood that complementary devices are also possible wherein each conductivity type is reversed.

Also, the cross-sections shown here are not drawn 35 to scale but are intended to be illustrative. While the various transistor doped regions shown here are

conventionally delineated by lines, this is also illustrative rather than representative. In the figures, identical reference numbers used in various figures denote similar structures. Also, the various 5 parameters disclosed herein for thickness, depths, widths, doping concentrations, dosages, and implantation energies are illustrative rather than limiting. Also, various materials may be used for the positive and negative type dopants. While the 10 substances conventionally used for these dopant types may be used, this is not limiting.

The top side geometries for the various transistors herein are not depicted since these are conventional in terms of the cell arrangement and 15 terminations. The terminations are generally not shown here but are e.g. those conventionally used with DMOSFETs.

Figure 2 therefore shows in cross-section one cell (and a portion of adjoining cells) of the present 20 transistor which includes drain region 50 N+ doped to a resistivity of e.g. 1 to 5 milliohm•cm and having a conventional thickness. Conventionally a metallized drain electrode 80 is formed on the bottom surface of this drain region 50 as an electrical contact thereto. 25 Formed on the drain region 50 (substrate) is an N- doped (e.g. epitaxial) layer (this need not be an epitaxial layer but is conventionally so formed) which typically has a resistivity of 0.3 to 1.0 ohm•cm. The N- doped portion 54 of the epitaxial layer is 30 conventionally referred to as a drift region. The epitaxial layer has a total thickness (extending to the principal surface of the transistor structure) of e.g. 8 to 12 μ m.

A P doped body region 56 is formed in the upper 35 portion of the epitaxial layer. A typical dopant level of the body region 56 at the principal surface is 5 x

10¹⁵/cm³. Included as part of body region 56 is a lower deep body P+ doped portion 57 having a total depth from the principal surface of the semiconductor body of about 2.5μm and extending below the bottom of the 5 trenches as shown. A typical doping level of the deep body P+ portion 57 is 2 × 10¹⁹/cm³.

Penetrating from the principal surface of the semiconductor body into the drift region 54 is a set of trenches which defines the transistor cells. (Only one 10 such trench 62 is shown here, in cross-section.)

Trench 62, as are the other trenches, is lined with gate oxide layer 66 which is typically 0.05 to 0.07μm thick, and each trench 62 is then filled with a conductive doped polysilicon gate electrode 64. A 15 typical width of trench 62 is 0.8 to 1.0μ. A typical cell pitch is 6.0μ. A typical depth of trench 62 is 1 to 2μm (less than that of deep body portion 57). Typically therefore the P+ deep body portion 57 extends 0.5μm below the bottom (floor) of the trench 62.

20 Formed in the upper portion of the epitaxial layer are N+ doped source regions 58, having a typical depth of 0.5μ. A typical doping level of the N+ source regions 58 is 6 × 10¹⁹/cm³ at the principal surface.

Penetrating through the middle of each source region 58 25 is the trench 62 in which is formed the conductive electrode gate 64. Insulating the upper portion of each conductive gate electrode 64 is a BPSG (boro-phosphosilicate glass) insulating layer 74 formed over gate electrode 64. Contacting the source regions 58 30 and body regions 56 is a source-body metallization layer 76.

The depiction herein is of the active portion only of the transistor. Each transistor active portion is typically surrounded by a termination, typically 35 including doped regions and sometimes an additional filled-in trench. Conventional terminations are

suitable in accordance with the present invention and hence the termination is not illustrated or described further herein.

A feature of the structure of Figure 2 in
5 accordance with the present invention is the trench bottom implant region 70, which is N doped to a concentration in a range of e.g. 1×10^{16} to $8 \times 10^{16}/\text{cm}^3$. Intentionally, the trench bottom implant region 70 is of higher doping concentration than is the surrounding
10 drift region 54 but of much lower doping concentration than drain region 50. Trench bottom implant region 70 advantageously eliminates the above-described parasitic JFET, which in prior art MOSFETS appears between deep body P+ regions at the trench bottoms. Region 70 as
15 shown extends as deep into drift region 54 as does the lowest part of deep body region 57, in this embodiment. The parasitic JFET resistance is thereby significantly reduced. Breakdown at the corners of the trench due to the local electric field concentration is also
20 prevented by optimizing the implant dose.

Also, unlike the prior art planar transistor of Lidow et al., there is no punchthrough problem since there is no additional doping added in the channel region between the source and body regions. In the
25 planar transistor structure of Lidow et al., there is an enhanced chance of lateral punchthrough from source regions 32 and 33 through the respective body regions

34 and 35. Such punchthrough would occur at the principal surface of the P body regions 34 and 35. Thus in the structure of Figure 2, the blocking characteristics are not degraded while advantageously 5 the on-resistance is reduced.

The typical thickness (height) of the trench bottom implant region 70 is 0.5μ . The width is typically that of the trench, i.e. it extends from one side of the trench to the other including the trench 10 corners, and extends a slight distance laterally from the trench corners, as a result of its fabrication by diffusion. A typical distance from the bottom portion of trench bottom implant region 70 to the substrate 50 is $1.0\mu\text{m}$, but this distance is not limiting; trench 15 bottom implant region 70 can extend to substrate 50.

An exemplary process flow for fabricating the transistor of Figure 2 is described hereinafter. It is to be understood that this process flow is not the only way to fabricate the structure of Figure 2, but is 20 illustrative. The various parameters given herein may be varied and still be in accordance with the present invention.

One begins as shown in Figure 3A with an N+ substrate 50 conventionally doped to have a resistivity 25 in the range described above. An epitaxial layer 54 is then grown thereon having a higher resistivity (as described above) and a thickness of e.g. 6 to $12\mu\text{m}$.

The principal surface of the semiconductor body including the epitaxial layer 54 then has a 30 conventional active mask layer (not shown) formed thereon and patterned. This active mask layer may be oxide or other suitable material, and defines the active portion of the transistor and masks off the termination thereof. It is to be understood that the 35 present figures show only the active portion, with the termination not being shown as being outside the area

of the drawings.

Next (see Figure 3B) a P+ region mask layer (not shown) is formed and patterned, masking off all portions of the principal surface of the semiconductor body except for where the P+ deep body portions (tubs) 57 are to be formed. After patterning this mask layer, a P+ solid source diffusion is performed using boron nitride. Hence the P+ dopant is boron; the diffusion 57 is to a depth of about 1.5 μ m.

10 A trench mask layer (not shown) is then formed and conventionally patterned. Using the trench mask layer as a pattern, the trenches are then anisotropically etched. The trenches, e.g. trench 62, are then subject to a sacrificial oxide step to smooth their sidewalls 15 and bottoms. This sacrificial oxide step involves growing a layer of oxide and then removing it by etching. The gate oxide layer 66 is then grown conventionally, as shown in Figure 3B, to a thickness of e.g. 0.05 to 0.07 microns.

20 Then in a departure from the conventional process flow and as shown in Figure 3C, a blanket N ion implant is carried out over the entire principal surface and into the trench 62. This is a vertical implant at an angle directly perpendicular to the plane defined by 25 the principal surface of the semiconductor body. The implant energy is e.g. in the range of 30 to 100 KeV and a dose of 10¹² to 10¹³/cm².

30 This trench bottom implant step results in the formation of an N doped region 70 at the bottom of trench 62, and also the formation of corresponding N doped regions 80 extending from the principal surface.

35 Then as shown in Figure 3D, a layer of polysilicon 64 is formed on the principal surface of the semiconductor body and filling the trench 62. This polysilicon layer is doped with an N type dopant to achieve maximum conductivity.

Then conventionally a gate mask layer (polymask) is formed over the entire surface of the polysilicon layer and patterned. (This step is not depicted.) This gate mask layer is then used to etch away the 5 polysilicon layer 64, except in the trench 62, and also leaving gate contact fingers (not shown) on the principal surface connecting the gate electrodes in the various trenches.

Then a blanket P-type implant forms the P doped 10 body regions 56 to provide a channel alongside the trench sidewalls. This step uses a dosage of e.g. 10^{13} to 10^{14} per/cm² and an energy of 50 to 60 KeV, typically using boron as the dopant for an N channel device.

As depicted in Figure 3D, the combined effects of 15 the P body implant 56 and the P+ tub 57 effectively eliminate the N doped regions 80 of Figure 3C.

Then an N+ source region mask layer is formed and patterned to define the N+ source regions 58. The N+ source region implant is then performed at an energy 20 level of e.g. 60 to 100 KeV at a dosage of 5×10^{15} to 8×10^{15} /cm², the dopant being arsenic. The N+ source mask is then stripped.

Next, a layer of borophosphosilicate glass (BPSG) is conventionally formed (not shown) to a thickness of 25 1 to 1.5 μm . A BPSG mask layer is then formed and patterned over the BPSG layer, and then the BPSG mask layer is used to etch the BPSG, defining BPSG region 74 of Figure 2 insulating the top side of conductive gate electrode 64.

30 Then conventional steps are used to complete the device, i.e. stripping the BPSG mask layer, depositing the source-body metal layer, and masking the metal layer to define the source-body contact 76 of Figure 2. Then a passivation layer is formed thereover and a pad 35 mask is formed thereon and patterned to define the pad contacts through the passivation layer. The formation

of the metal layer 76 has a corresponding step to form the contact 80 (see Figure 2) to the drain layer 50 on the backside of the substrate.

This disclosure is illustrative and not limiting;
5 further variations and modifications will be apparent to one skilled in the art in light of this disclosure and are intended to fall within the scope of the appended claims.

We claim:

1. A transistor structure comprising:
 - a substrate of a first conductivity type;
 - a drift region overlying the substrate and of the first conductivity type and doped to a concentration less than that of the substrate;
 - a body region of a second conductivity type opposite that of the first conductivity type overlying the drift region, and defining a principal surface of the transistor structure;
 - a conductive gate electrode extending in a trench from the principal surface through the body region and into the drift region to a depth less than that of the body region;
 - a source region of the first conductivity type extending into the body region from the principal surface; and
 - a trench bottom region of the first conductivity type and of a higher doping concentration than the drift region, and extending from a bottom of the trench into the drift region.
2. The transistor structure of Claim 1, wherein the trench bottom region has a doping concentration in a range of $1 \times 10^{16}/\text{cm}^3$ to $8 \times 10^{16}/\text{cm}^3$.
3. The transistor of Claim 1, wherein the trench bottom region has a doping concentration at least four times that of the drift region.
4. The transistor structure of Claim 1, wherein the body region includes a channel portion in contact with a side of the trench near the principal surface, and a deep body portion more heavily doped than the channel portion and spaced apart from a side of the trench and nearer the bottom of the trench than is the

channel portion.

5. The transistor structure of Claim 4, wherein
the trench bottom region is spaced apart from the deep
5 body portion.

6. The transistor structure of Claim 1, wherein
the trench bottom region extends at least $0.5\mu\text{m}$ into
the drift region from the bottom of the trench.

10

7. The transistor structure of Claim 1, wherein
the trench bottom region is spaced apart from the
substrate by at least $1\mu\text{m}$.

15

8. A method of forming a transistor structure,
comprising the steps of:

providing a substrate of a first conductivity
type;

20

forming a drift region on an upper portion of
the substrate, the drift region being of the first
conductivity type and doped to a concentration
lower than that of the substrate;

25

forming a body region of a second
conductivity type opposite to the first
conductivity type and extending from a principal
surface of the drift region into the drift region;

30 forming a trench extending into the drift
region to a depth less than that of the body
region;

35

implanting through a bottom of the trench,
and into the drift region, a trench bottom region
of the first conductivity type and having a doping
concentration greater than that of the drift
region;

35

filling the trench with a conductive gate
electrode, after the step of implanting the trench

bottom region; and
forming a source region of the first conductivity type and extending into the body region from the principal surface.

5

9. The method of Claim 8, further comprising the steps of:

after forming the trench, and before the step of implanting, forming an oxide layer lining the trench; and

10 etching away at least a predetermined thickness of the oxide layer.

15 10. The method of Claim 8, wherein the step of implanting comprises implanting negatively charged ions at an energy in a range of 30 to 100 KeV, and a dose of 10^{12} to $10^{13}/\text{cm}^2$.

20 11. The method of Claim 8, wherein the step of implanting comprises directing ions at an angle of 90° to a plane defined by the principal surface.

25 12. The transistor structure of Claim 8, wherein the trench bottom region has a doping concentration in a range of $1 \times 10^{16}/\text{cm}^3$ to $8 \times 10^{16}/\text{cm}^3$.

13. The transistor of Claim 8, wherein the trench bottom region has a doping concentration at least four times that of the drift region.

30

14. The transistor structure of Claim 8, wherein the step of forming a body region comprises:

forming a channel portion in contact with a side of the trench near the principal surface; and

35 forming a deep body portion spaced apart from a side of the trench and near the bottom of the trench.

15. The transistor structure of Claim 14, wherein
the trench bottom region is spaced apart from the deep
body portion.

5 16. The transistor structure of Claim 8, wherein
the trench bottom region extends at least $0.5\mu\text{m}$ into
the drift region from the bottom of the trench.

10 17. The transistor structure of Claim 8, wherein
the trench bottom region is spaced apart from the
substrate by at least $1\mu\text{m}$.

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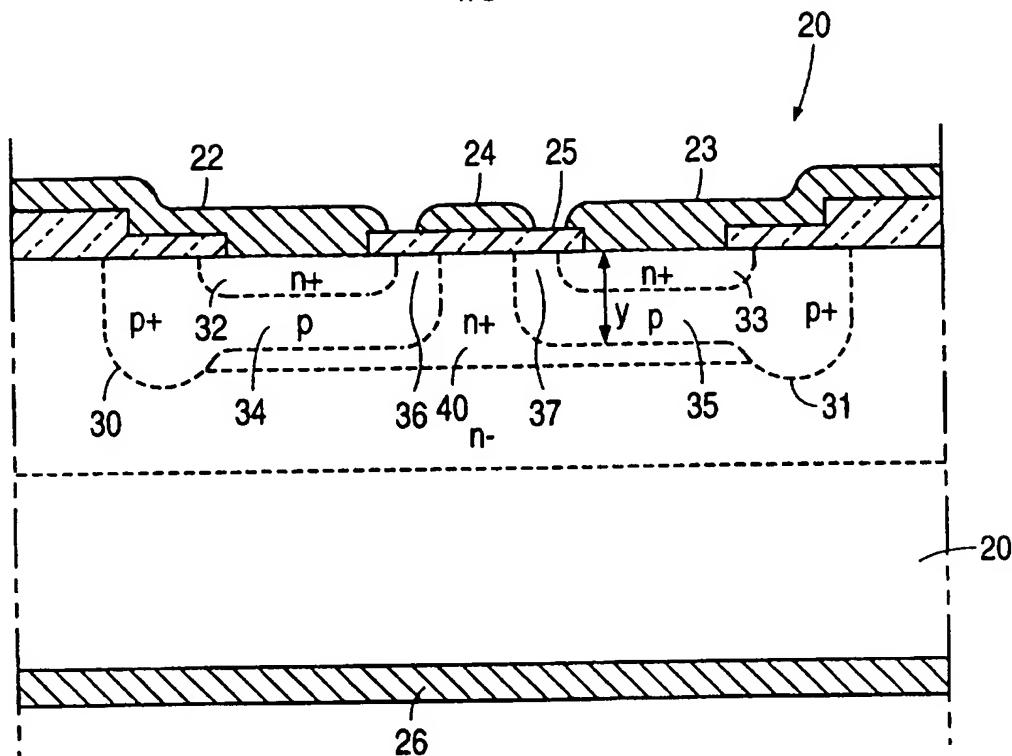


FIG. 1
(PRIOR ART)

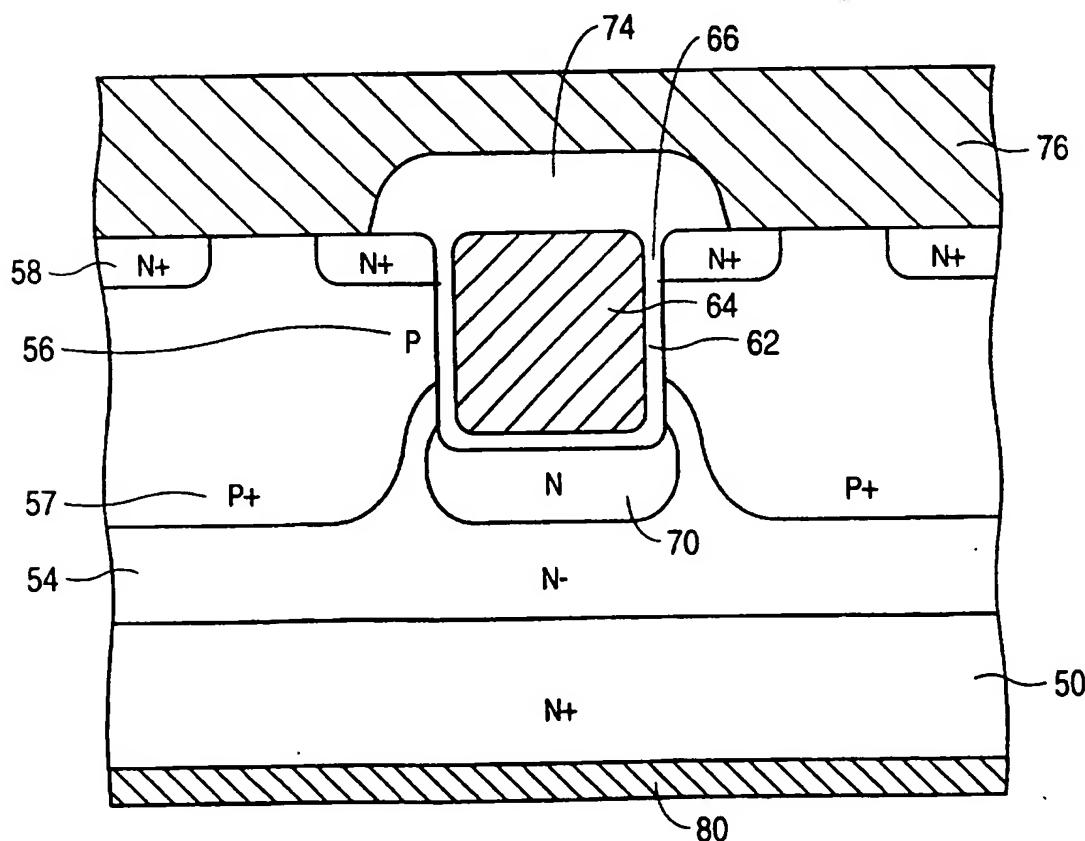


FIG. 2

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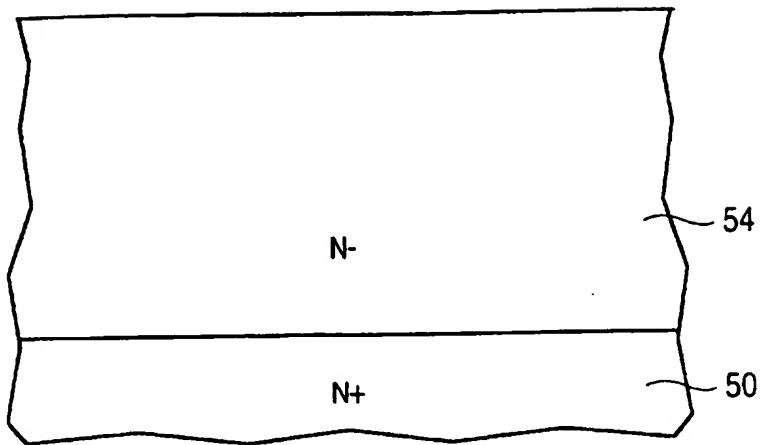


FIG. 3A

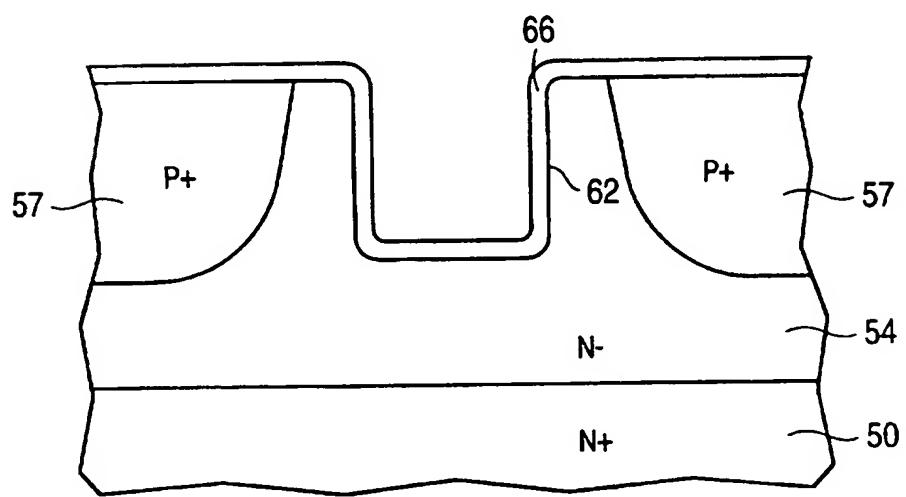


FIG. 3B

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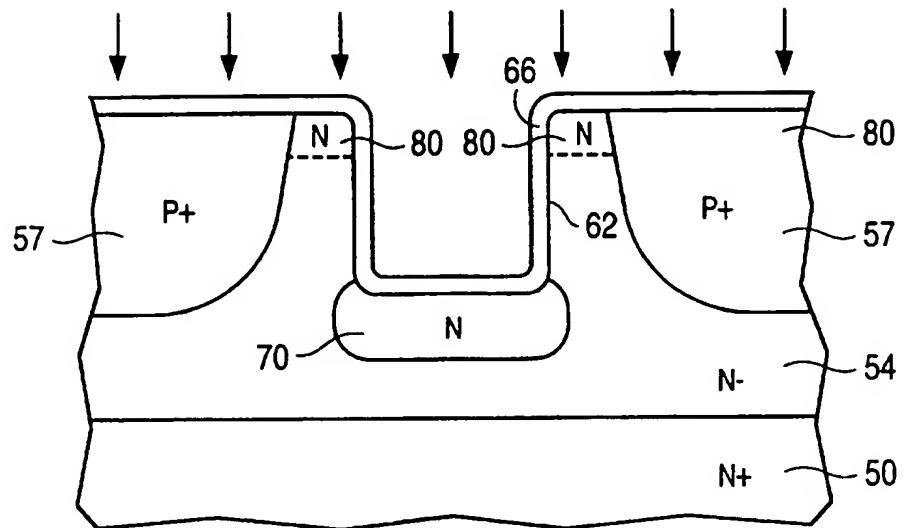


FIG. 3C

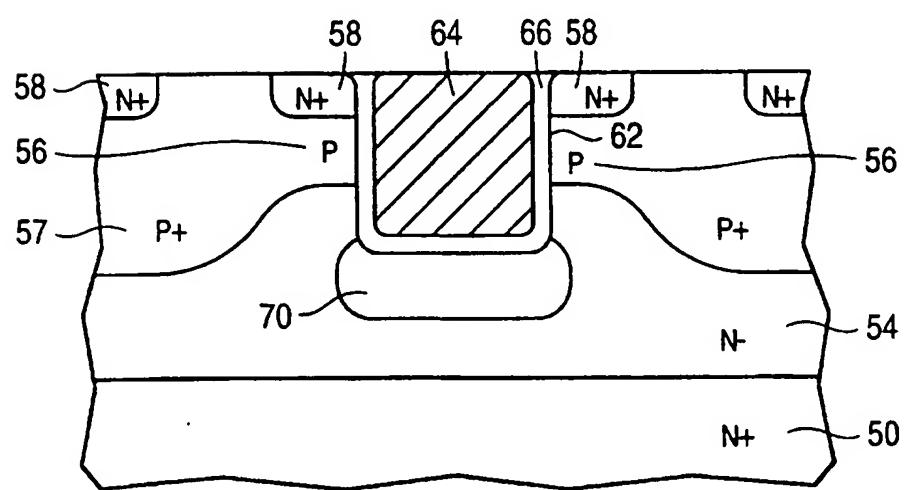


FIG. 3D

INTERNATIONAL SEARCH REPORT

International application No.

PCT/US97/12046

A. CLASSIFICATION OF SUBJECT MATTER

IPC(6) :H01L 29/76

US CL :257/328, 329, 330

According to International Patent Classification (IPC) or to both national classification and IPC

B. FIELDS SEARCHED

Minimum documentation searched (classification system followed by classification symbols)

U.S. : 257/328, 329, 330

Documentation searched other than minimum documentation to the extent that such documents are included in the fields searched

Electronic data base consulted during the international search (name of data base and, where practicable, search terms used)

C. DOCUMENTS CONSIDERED TO BE RELEVANT

Category*	Citation of document, with indication, where appropriate, of the relevant passages	Relevant to claim No.
Y	US 5,442,214 A (YANG) 15 AUGUST 1995 (15/08/95). COLUMN 3, LINES 1-68.	8-11
Y, P	US 5,558,313 A (HSIEH ET AL.) 24 SEPTEMBER 1996 (24/09/96), COLUMN 4, LINES 38-67.	1-7, 12-17
Y	US 4,893,160 A (BLANCHARD) 09 JANUARY 1990 (09/01/90). COLUMN 3, LINES 9-23.	8-11
Y	US 4,984,080 A (TZENG) 16 OCTOBER 1990 (16/10/90). COLUMN 6, LINES 35-68.	1-7, 12-17
Y	JP 405,343,691 A 24 DECEMBER 1993 (24/12/93). CONSTITUTION.	1-7, 12-17

 Further documents are listed in the continuation of Box C. See patent family annex.

* Special categories of cited documents:	"T"	later document published after the international filing date or priority date and not in conflict with the application but cited to understand the principle or theory underlying the invention
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P document published prior to the international filing date but later than the priority date claimed		

Date of the actual completion of the international search	Date of mailing of the international search report
02 OCTOBER 1997	13 OCT 1997
Name and mailing address of the ISA/US Commissioner of Patents and Trademarks Box PCT Washington, D.C. 20231 Facsimile No. (703) 305-3230	Authorized officer IDA MARIE SOWARD Telephone No. (703) 308-4889

INTERNATIONAL SEARCH REPORT

International application No.

PCT/US97/12046

Box I Observations where certain claims were found unsearchable (Continuation of item 1 of first sheet)

This international report has not been established in respect of certain claims under Article 17(2)(a) for the following reasons:

1. Claims Nos.:
because they relate to subject matter not required to be searched by this Authority, namely:

2. Claims Nos.:
because they relate to parts of the international application that do not comply with the prescribed requirements to such an extent that no meaningful international search can be carried out, specifically:

3. Claims Nos.:
because they are dependent claims and are not drafted in accordance with the second and third sentences of Rule 6.4(a).

Box II Observations where unity of invention is lacking (Continuation of item 2 of first sheet)

This International Searching Authority found multiple inventions in this international application, as follows:

Please See Extra Sheet.

1. As all required additional search fees were timely paid by the applicant, this international search report covers all searchable claims.
2. As all searchable claims could be searched without effort justifying an additional fee, this Authority did not invite payment of any additional fee.
3. As only some of the required additional search fees were timely paid by the applicant, this international search report covers only those claims for which fees were paid, specifically claims Nos.:

4. No required additional search fees were timely paid by the applicant. Consequently, this international search report is restricted to the invention first mentioned in the claims; it is covered by claims Nos.:

Remark on Protest

The additional search fees were accompanied by the applicant's protest.

No protest accompanied the payment of additional search fees.

INTERNATIONAL SEARCH REPORTInternational application No.
PCT/US97/12046**BOX II. OBSERVATIONS WHERE UNITY OF INVENTION WAS LACKING**

This ISA found multiple inventions as follows:

This application contains the following inventions or groups of inventions which are not so linked as to form a single inventive concept under PCT Rule 13.1. In order for all inventions to be searched, the appropriate additional search fees must be paid.

Group I, claim(s) 1-7 and 12-17, drawn to a device, class 257, subclass 328.
Group II, claim(s) 8-11, drawn to a method, class 438, subclass 15+.

The inventions listed as Groups I and II do not relate to a single inventive concept under PCT Rule 13.1 because, under PCT Rule 13.2, they lack the same or corresponding special technical features for the following reasons: unpatentability of the group I invention would not necessarily imply unpatentability of the group II invention could be made by processes materially different from those of the group II invention. For example, diffusing through a bottom of the trench instead of implanting through a bottom of the trench may be performed and the same structure would result.